In the context of integrated circuits, NMOS and PMOS transistors are combined in close proximity to form *complementary-MOS*, or CMOS, circuits. CMOS circuits are dense, consume relatively little power, and are easily fabricated on a silicon chip. As with any real-world device, FETs contain parasitic properties, including capacitance between the gate and the source and drain, C_{GS} and C_{GD}. This capacitance, although small, imposes a load on the circuit that drives the gate during switching. However, when a FET is held static, such as in a DC or low-frequency circuit, the load on the driving circuit is essentially zero.

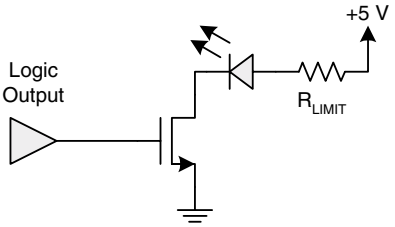

FIGURE 13.22 NMOS transistor LED driver.

The 2N7002, a widely available FET, can be connected to drive a load as shown in Fig. 13.22 using the previous LED example. A gate resistor is not needed, because there is no DC path to limit the current through. An appropriate current limiting resistor in the load's path may or may not be required. If the 2N7002's $I_{DS\ (MAX)}$ at the driven V_{GS} is within the load's specifications, the FET will serve as the current limiting element. A logic output, especially one operating at a low voltage (e.g., 3.3 V or less) may not provide sufficient V_{GS} to drive a heavy load. This must be verified ahead of time using manufacturers' data sheets.

Aside from the terminal capacitances already mentioned, FETs contain other parasitic characteristics that must be taken into account when designing certain types of circuits. One such characteristic develops when the FET's *body*, the silicon that forms the channel and that surrounds the source and drain regions, is kept at a voltage that differs from that of the source. A typical discrete FET does not suffer this problem, because the body and source are electrically connected within the package. ICs, however, consist of thousands or millions of FETs wherein the bodies of each FET are not all at the same voltages as their associated sources. This voltage, V_{BS}, degrades the ability of the channel to conduct current and causes a FET's V_T to increase, requiring a higher V_{GS} to conduct. More complete graphical representations of NMOS and PMOS FETs are shown in Fig. 13.23. Unlike the representations shown thus far, these explicitly show the FET's body. A discrete FET usually has its body and source connected as shown. For the sake of simplicity, many circuit diagrams showing discrete FETs use the basic representation, because it is known that $V_{BS} = 0$.

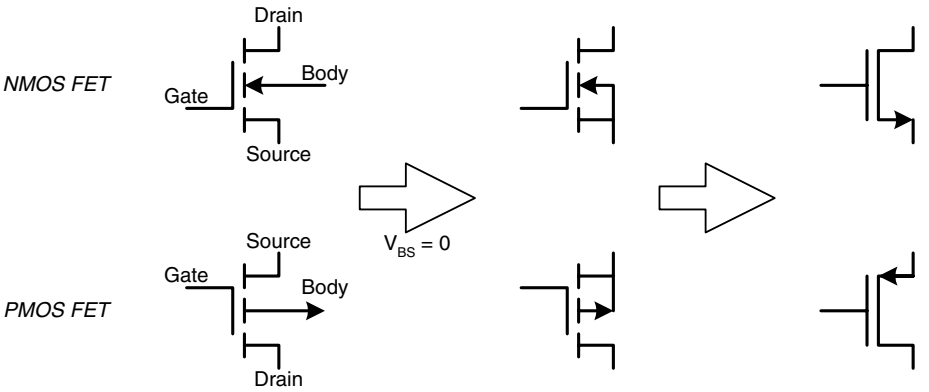

FIGURE 13.23 Graphical representation of FET body.

13.8 POWER FETS AND JFETS

Discrete FETs are used in a variety of applications. In digital systems, FETs are often found in power supply and regulation circuitry because of the availability of low-resistance devices. A key parameter of a FET used in power applications is its channel resistance between the source and drain, R_{DS}. Per the basic power relationship, $P = I^2R$, a FET with low R_{DS} will waste less power and will therefore operate at a cooler temperature. Power FET circuits can either handle more current without overheating or can be made to run cooler to extend their operational life span. It is not difficult to find power FETs with R_{DS} well below 10 mΩ. In contrast, a BJT exhibits a $V_{CE\ (SAT)}$ that dissipates significant power at high currents (P = IV). The saturation voltage also increases with I_C, causing more power to be dissipated in high-power applications.

When FETs are constructed as part of an IC, they are built in a lateral configuration atop the silicon substrate with a structure similar to what was shown earlier. Discrete FETs, however, are often constructed in a vertical manner known as *double-diffused MOS*, or DMOS, where the source and drain are on opposite sides of the silicon chip. The DMOS structure is shown in Fig. 13.24. DMOS surrounds the source with a thin region of oppositely doped silicon that serves as the body through which the conducting channel is induced by a voltage applied to the gate. Around the body is the substrate, which is doped similarly to the drain. Discrete FETs are constructed in this manner, because the thin channel between the source and the substrate provides low R_{DS} and, consequently, high current capacity with reduced power dissipation.

DMOS FETs are constructed in a manner that electrically connects the source and body regions, as shown by the metal source contacts in Fig. 13.24, so that a parasitic NPN transistor does not arise and cause problems. A consequence of this technique is that a parasitic diode is formed between the body and drain. Because the body is connected to the source, this is actually a source-drain diode with the anode at the source and the cathode at the drain for an n-FET. The diode is reverse biased under most conditions, because an n-FET's source is usually at a lower voltage than the drain. Therefore, V_{DS} would have to approach –0.6 V for conduction to occur. Figure 13.24 also shows the graphical representation of an n-type DMOS transistor with a source-drain diode. If an n-FET is designed such that the source is always connected to ground and the drain can never drop below 0 V, the diode has no effect. In less obvious configurations, the biasing of this inherent diode should be taken into account to ensure that current does not flow through an unintended path.

A potentially dangerous characteristic of FETs is a consequence of the insulated gate's high input impedance. If a FET circuit does not create a path to the gate through which stray electrical charge can drain away, a high voltage can build up and cause permanent damage to the device. The gate is a small capacitor, and it is known that $V_{CAP} = Q \div C$. Therefore, a small charge accumulating on a very

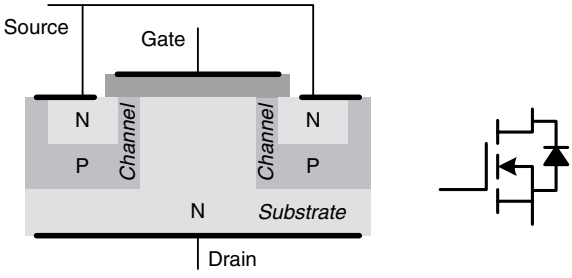

FIGURE 13.24 DMOS n-FET simplified structure and graphical representation.